TIMING ANALYSIS AND OPTIMIZATION OF SEQUENTIAL CIRCUITS

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Analysis and Optimization of Sequential Circuit Elements to Combat Single-Event Timing Upsets. Hamed Abrishami, Safar Hatami, and Massoud Pedram.

Almost all static timing analysis techniques used today for evaluating timing performance of sequential circuits are based on setup and hold.

Timing analysis and optimization of sequential circuits

Sequential Circuit. ? Arrival times . ?identify critical paths for performance optimization - don't want to try to ?Perform timing analysis of a gate-level circuit.

Naresh Maheshwari (Author of Timing Analysis and Optimization of Sequential Circuits)

other optimization techniques. In Chapter 5, we consider retiming under both setup and hold constraints. Given an edge-triggered sequential circuit G = (V,E), .

Neglect the short path constraints (which may be nonconvex [Fis90) and solve the combined sizing and skew optimization under long path constraints only.

Naresh Maheshwari is the author of Timing Analysis and Optimization of Sequential Circuits (avg rating, 0 ratings, 0 reviews, published).

synchronous sequential circuit area optimization problem and present the .. For each PO which violates the timing constraints, we identify the longest path.

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Circuit transformation from gate level to a graph model, which has vertices and edges to represent the gates and the connections, is straightforward. After Appling this algorithm on G cthe purpose of G c is gained and the C L is calculated for every transistor in the input circuit. IfthepathslackSPispositivethenthatmeansthatthesignalthatwaslaunch In this case, the algorithm checks the w; if v and w have same type ex. Note that this is non-obvious because pre-CTS circuit optimization normally would not try to increase the positive slack of a timing path. TheGcisdirectgraphconsistfromsetofverticesVcandsetofedgesEcwheree is also capable to show the effects of changing the sizing of the transistors that are located in the non-critical path in saving the leakage power for the circuit. However, in some embodiments, the timing paths irrespective of their slacks can be prioritized based on how many negative slack super paths share a given timing path.